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EXAMINER	
PRINCE, JESSICA MARIE	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.**	**Applicant(s)**	
	10/817,380	THANGARAJ ET AL.	
	Examiner	**Art Unit**	
	JESSICA PRINCE	2482	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 19* is/are rejected.

7)☒ Claim(s) *14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

Claims 1-15 and 19 are presently pending and claims 16-18 are cancelled; claim 19 has been added by Applicants amendment filed 09/21/2010.

Acknowledgment of Amendment

Applicant's amendment filed on 09/21/2010 overcomes the following objection(s)/rejection(s):

The objection to claim 14 has been withdrawn in view of Applicants amendment.

Response to Arguments

Applicants' argument regarding that there is no teaching that the byte is "in a middle portion of a data word". Moreover, [0123] teaches that "Fig. 14 shows a real example of a header of an MPEG stream". Note that since Figure 14 merely describes the stream, without any reference to how the stream is stored in memory, the foregoing does not teach "a start code starting at a byte in the middle portion of a data word in a memory".

The Examiner respectfully disagrees. Sugiyama teaches where in fig. 13A, in each of the higher layers from the sequence layer to the picture layer, each code boundary is byte assigned. In the slice layer, only the slice start code 12 is byte assigned, whereas each macroblock can be bit assigned as shown in fig. 13B. Further, fig.14 is a diagram showing a real example of a header of an MPEG stream according to a first embodiment, ([0052] and [0122]). A stream that is output from the selector 306

is temporality written into a memory 307 and a memory 313. The variable length code encoder (VLC) 3087 controls the address of the stream written in memory 307 so as to convert the stream into an MPEG stream, [0277]. Since the start codes are byte assigned and the header of the MPEG stream containing the start codes are written into a memory, clearly Sugiyama is fully capable of assigning the byte to a middle portion of the data word in MPEG stream written into a memory, which reads upon the claimed limitation.

As to Applicants argument that figures 13A and 14 are not mapped to memory. As to Applicants argument that even if what is depicted in Fig. 14 is stored in memory, Sugiyama does not store it consecutively. Thus, even if the byte assignment taught a start code in the middle of a data word, it does not follow that Sugiyama teaches storing the same in the middle of a memory word.

The examiner respectfully disagrees. The examiner respectfully disagrees and directs the Applicant to the response provided above. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., storing byte assignment consecutively and storing the byte assignment in a memory word) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al., US-5, 815,206 in view of Hrusecky et al., US-5,973,740 in view of Sugiyama et al., US- US-2003/00009722 and in further view of AAPA (herein referenced as Applicants Admitted Prior Art).

Regarding claim 1, Malladi teaches A method for decoding video data, said method comprising: writing a starting address associated with the byte in a table by said transport processor (column 4 line 25-29 and fig. 4); fetching data from the memory starting from the byte (column 15 line 39-41 and fig. 4) by a video decompression engine, said video decompression engine <u>decompressing</u> the data from the memory starting from the byte in the middle portion of the data word, thereby resulting in

decompressed video data; and writing the decompressed video data to a frame buffer (Fig. 4 is a schematic diagram illustrating the hardware layout and signal interfaces of an audio and video decoder designed in accordance with one embodiment, col. 14 line 56-59 and fig. 4). Malladi is silent in regard to writing a start code starting at a byte in a middle portion of a data word in a compressed data buffer memory; and fetching data from the memory starting from the byte in the middle portion of the data word by a video decompression engine, said video decompression engine decompressin the data from the memory starting from the bye in the middle portion of the data word, thereby resulting in decompressed video data.

However, Hrusecky teaches fetching data from memory by a video decompression engine (Fig. 4 clearly discloses where the video decoder (54) fetches data from the DRAM (53) using the memory controller (52), fig. 4 elements 52, 53, 54), said video decompression engine (fig. 4 element 54) decompressin the data from the memory (MPEG compressed video data is then retrieved by the video decoder 54 from the DRAM 53 and decoded, col.8 line 42-45) thereby resulting in decompressed video data (fig. 4) and writing the decompressed video data to a frame buffer (col. 8 line 45-49).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Hrusecky with Malladi for providing improved memory management.

Malladi (modified by Hrusecky) as a whole is silent in regards to writing a start code starting at a byte in a middle portion of a data word.

However, Sugiyama teaches to writing a start code starting at a byte in a middle portion of a data word in a memory (Sugiyama teaches fig. 14 is a schematic diagram showing a real example of a header of an MPEG stream according to a first embodiment, [0052]. Further disclosed is that a stream that is output from the selector 306 is temporally written to a memory 307 and a memory 313. The variable length code encoder (VLC) 308 controls the addresses of the stream written in the memory 307 so as to convert the stream into an MPEG stream, [0277]. Since Sugiyama discloses the stream can be written in the memory and the VLC controls the address of the stream, it is clear to the examiner that Sugiyama discloses the stream is written to an address in memory. Therefore, since Sugiyama discloses the start codes are byte assigned and the streams can be written in the memory and VLC controls the address of the stream, it is clear to the examiner Sugiyama disclose the writing a start code in the middle portion of a data word in memory, reading upon the claimed limitation); and fetching data from the memory starting from the byte in the middle portion of the data word (Sugiyama teaches writing the start code to a middle portion of a data word, (Sugiyama teaches fig. 14 is a schematic diagram showing a real example of a header of an MPEG stream according to a first embodiment, [0052]. Further disclosed is that a stream that is output from the selector 306 is temporally written to a memory 307 and a memory 313. The variable length code encoder (VLC) 308 controls the addresses of the stream written in the memory 307 so as to convert the stream into an MPEG stream, [0277]). Malladi teaches writing a starting address associated with the byte in the table (writing to a start code table, column 4 line 25-30) and fetching data from the memory starting from the

byte (once the start code table has the identifying stamp information, a CPU will periodically poll the start code table by communicating through a BIU that is connected with stream interface, column 15 line 39-41)).

Since Malladi writes and fetches (polls) to the start code table, which would include the address (or location) of the start code and Sugiyama writes to the start code to a middle portion of the data word, it is clear to the examiner that Malladi (modified by Sugiyama) is fully capable of fetching the start code from the byte in the middle of the data word, which reads upon the claimed limitation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Malladi with Sugiyama to provide a stream processing apparatus that stably operates even if an invalid VLC that is not contained in a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

Malladi (modified by Hrusecky and Sugiyama) is silent in regards to a compressed data buffer, a transport processor.

However, AAPA teaches a compressed data buffer (AAPA discloses that when a decoding system received video data for decoding, the decoding system places the video data in to a decompressed data buffer, [0005]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of AAPA with Malladi (modified by Hrusecky and Sugiyama) for providing improved image processing.

Regarding claim 2, Malladi (modified by Hrusecky, Sugiyama, AAPA) as a whole teaches everything claimed as applied above (see claim 1). In addition, Malladi teaches wherein the start code is associated with a slice (Malladi, column 8 line 32-34).

Regarding claim 3, Malladi (modified by Hrusecky, Sugiyama, and AAPA) as a whole teaches everything claimed as applied above (see claim 1). Sugiyama further teaches wherein the data word comprises at least 16 bytes (Sugiyama, fig. 14). Therefore, it would have been obvious for one of ordinary skill I the art at the time of the invention to combine the teaching of Malladi (modified by Hrusecky and AAPA) with Sugiyamas' teaching of a data word of at 16 bytes to provide a stream processing apparatus that stably operates even if an invalid VLC that is not contained in a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

Regarding claim 4, Malladi (modified by Hrusecky, Sugiyama, and AAPA) as a whole further teach writing another start code to another byte (Malladi teaches more than one start code, column 10 line 63-65) in a middle portion of another data word in the memory (Sugiyama, fig. 14); writing another address associated with the another byte in the table (Malladi, column 10 line 60-67); and wherein fetching data from the memory starting from the byte further comprises: fetching data from the memory starting from the byte and ending with a byte preceding the another byte (Malladi, column 15 line 39-41. It would be obvious that the system as disclosed by Malladi would be fully capable of fetching data from the memory starting from the byte and ending with a byte preceding the another byte, as the system checks for another start code (column 10 line

66-67), and if there is no start code, the process simply returns to decoding macroblocks as indicated (column 11 line 1-2). Further, the examiner notes that the byte at the end of the start code would be the byte preceding another start code.

Regarding claim 5, Malladi (modified by Hrusecky, Sugiyama, and AAPA) as a whole further teaches looking up the address in the table (Malladi teaches writing to the start code table, column 4 line 25-29. The examiner notes that since Malladi teaches writing to the start code table, it is clear that in order for Malladi to use the start codes, it would necessitate looking up the address from the start code table).

Regarding claim 6, Malladi (modified by Hrusecky, Sugiyama, and AAPA) as a whole further teaches where looking up the another address in the table (Malladi teaches writing to the start code table, column 4 line 25-29 The examiner notes that since Malladi teaches writing to the start code table, it is clear that in order for Malladi to use the start codes, it would necessitate looking up the address from the start code table).

Regarding claim 7, Malladi teaches system for decoding video data (abstract and column 1 line 24-26), said system comprising: a memory comprising a plurality of data words (Malladi, start code table, fig. 4), for storing a start code (fig. 4); a table for storing a starting address associated with the byte (Malladi, fig. 4); and a direct memory access module for providing data from the memory starting from the starting address (Malladi, column 21-24). Malladi is silent in regards to a compressed data buffer the start code starting at a byte in a middle portion of a particular one of the data words; the starting address in the middle portion of the data word; a video decompression engine for

decompressing the data from the memory starting from the starting address in the middle portion of the data word, thereby resulting in decompressed video data; and a frame buffer for storing the decompressed video data.

However, Hrusecky teaches a memory access module for providing data from a memory by a video decompression engine (Fig. 4 clearly discloses where the video decoder (54) has access to the DRAM by the memory controller (52) , fig. 4 elements 52, 53, 54) for decompressing the data from the memory (MPEG compressed video data is then retrieved by the video decoder 54 from the DRAM 53 and decoded, col.) thereby resulting in decompressed video data (fig. 4); and a frame buffer for storing the decompressed video data (fig. 5 element 107).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Hrusecky with Malladi for providing improved memory management.

Malladi (modified by Hrusecky) is silent in regards the start code starting at a byte in a middle portion of a particular one of the data words; the starting address in the middle portion of the data word.

However, Sugiyama teaches the start code starting at a byte in a middle portion of a particular one of the data words (fig. 14); the starting address in the middle portion of the data word (Sugiyama teaches fig. 14 is a schematic diagram showing a real example of a header of an MPEG stream according to a first embodiment, [0052]. Further disclosed is that a stream that is output from the selector 306 is temporally written to a memory 307 and a memory 313. The variable length code encoder (VLC)

308 controls the addresses of the stream written in the memory 307 so as to convert the stream into an MPEG stream, [0277]). Malladi teaches writing a starting address associated with the byte in the table (writing to a start code table, column 4 line 25-30) and fetching data from the memory starting from the byte (once the start code table has the identifying stamp information, a CPU will periodically poll the start code table by communicating through a BIU that is connected with stream interface, column 15 line 39-41)).

Since Malladi writes and fetches (polls) to the start code table, which would include the address (or location) of the start code and Sugiyama writes to the start code to a middle portion of the data word, it is clear to the examiner that Malladi (modified by Sugiyama) is fully capable of the starting the address in the middle portion of the data word.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Malladi with Sugiyama to provide a stream processing apparatus that stably operates even if an invalid VLC that is not contained in a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

Malladi (modified by Hrusecky and Sugiyama is silent in regards to compressed data buffer, a transport processor.

However, AAPA teaches a compressed data buffer (AAPA discloses that when a decoding system received video data for decoding, the decoding system places the video data in to a decompressed data buffer, [0005]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of AAPA with Malladi (modified by Hrusecky and Sugiymama) for providing improved image processing.

Regarding claim 8, Malladi (modified by Hrusecky, Sugiyama, and AAPA) as a whole teaches everything claimed as applied above (see claim 7). In addition, Malladi teaches a video transport processor (Malladi, fig. 4:417) for writing the start code starting at a byte in a middle portion of the particular data word in the memory (Sugiyama, fig. 14).

Regarding claim 9, Malladi (modified by Hrusecky, Sugiyama and AAPA) as a whole teaches everything claimed as applied above (see claim 7). In addition, Malladi wherein the start code is associated with a slice (Malladi, start code, column 8 line 32-34 and fig. 1A).

Regarding claim 10, Malladi (modified by Hrusecky, Sugiyama and AAPA) as a whole teaches everything claimed above (see claim 7). Malladi is silent in regards to the data word comprises at least 16 bytes.

However, Sugiyama teaches the data word comprises at least 16 bytes (Sugiyama, fig. 14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Malladi (modified by Hrusecky and AAPA) with Sugiyamas' teaching of the data word comprising at least of 16 bytes to provide a stream processing apparatus that stably operates even if an invalid VLC that

is not contained in a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

Regarding claim 11, Malladi (modified by Hrusecky, Sugiyama and AAPA) as a whole further teaches wherein the video transport processor (Malladi, fig. 4:417) writes another start code (Malladi, teaches more than one start code, column 10 line 63-65) in the memory and wherein the table stores another address associated with the another byte in the table (Malladi, start code table, fig. 4) and wherein the direct memory access module fetches data from the memory starting from the byte and ending with a byte preceding the another byte (Malladi, column 15 line 39-41. It would be clear that the system as disclosed by Malladi would be fully capable of fetching data from the memory starting from the byte and ending with a byte preceding the another byte, as the system checks for another start code (column 10 line 66-67), and if there is no start code, the process simply returns to decoding macroblocks as indicated (column 11 line 1-2). Further, it is clear that the byte at the end of the start code would be the byte preceding another start code). Malladi is silent in regards to another byte in a middle portion of another data word.

However, Sugiyama teaches another byte in a middle portion of another data word (Sugiyama, fig. 14)

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Malladi (modified by Hrusecky and AAPA) with Sugiyamas' teaching of a start code in the middle of a data word to provide a stream processing apparatus that stably operates even if an invalid VLC that is not contained in

a VLC table that is referenced when the VLC is decoded is input to a system that handles an MPEG stream (Sugiyama, [0032]).

Regarding claim 12, Malladi (modified by Hrusecky, Sugiyama, and AAPA) as a whole teaches everything claimed as applied above (see claim 7). In addition Malladi teaches a master processor for looking up the address in the table (Malladi, column 15 line 38-42).

Regarding claim 13, Malladi (modified by Hrusecky, Sugiyama, and AAPA) as a whole teaches everything claimed as applied above (see claim 7). In addition Malladi wherein the master processor looks up the another address in the table (Malladi, teaches writing more than one start code, column 10 line 60-67. The examiner notes, since Malladi writes more than one start code, and it polls the entire start code table, it is clear that more than one address is looked up, Malladi, column 15 lines 38-42).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al., US-5, 815,206 in view of Hrusecky et al., US-5,973,740 in view of Sugiyama et al., US-US-2003/00009722 and in view of AAPA (herein referenced as Applicants Admitted Prior Art) and in view of Son et al., US-5,898,897 and further in view of Foster et al., US-7,024,685.

Regarding claim 19, Malladi (modified by Hrusecky, Sugiyama and AAPA) as a whole teaches everything as claimed above, see claim 1. Malladi is silent in regards to

the method of claim 1, further comprising masking a portion of a first data structure that proceeds the starting address with a masking register.

However, Son teaches where the multi-standard start code detector system 300 of bitstream processor 234 beings searching for a next start code of compressed video bit stream 402 after either end of image data 408 is detected or any corrupted image data 408 is detected by DSP core 201 or bitstream processor 234. Upon beginning a next start code 405 detection operation to detect next start code 405, multi-standard start code detector system 300 rapidly discards entire bit groups until detection of at least a portion of next start code. This operation may be conducted on all of the byte aligned and non-byte aligned bitstream formats. Next start code detection operations involving non-byte aligned formats may involve a limited bit by bit discard. By discarding groups of bits rather than bit by bit, detection of start codes decreases and more processing time can be devoted to processing useful information, see col. 8 line 55-63. Son discloses to mask portions of image data until at least a portion of the next start code is detected.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Son with Malladi (modified by Hrusecky, Sugiyama, and AAPA) for providing improved

Malladi (modified by Hrusecky, Sugiyama, AAPA and Son) as whole is silent in regards to a masking register. However, Foster teaches a masking register (col. 12 line 31-36).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Foster with Malladi (modified by Hrusecky, Sugiyama, AAPA, and Son) to provide the ability to selectively mask bits.

Allowable Subject Matter

3. Claims 14-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter: The invention as claimed involves a system for decoding video data where the novel features include wherein the direct memory access module further comprises: a buffer comprising a plurality of data words for storing the video data from the starting address; a first masking register for discarding a portion of a first data structure that precedes the starting address, the first masking register comprises a plurality of bytes corresponding to byte positions; and a state machine for loading the first masking register with a pattern wherein each byte of the plurality of bytes in the first mask register that corresponds to a byte position that is less than the four least significant bits of the starting address are loaded with a first value, and wherein each byte of the plurality of bytes in the first mask register that corresponds to a byte position that is equal or greater than the four least significant bits of the starting address are loaded with a second value.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

/JESSICA (ROBERTS) PRINCE/

Examiner, Art Unit 2482

/Marsha D. Banks-Harold/

Supervisory Patent Examiner, Art Unit 2482